PID TUNING FOR DOMINANT POLES AND PHASE MARGIN

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ABSTRACT

A simple PID tuning method for dominant pole placement and phase margin specification is proposed in this paper. Time domain specifications as settling time and percentage overshoot are represented by a pair of dominant poles, which is combined with phase margin specification to achieve closed-loop stability and robustness. A graphical method is developed to determine PID settings to meet these specifications simultaneously. An example is given for illustration.

KeyWords: PID controller, dominant pole placement, phase margin, graphical method.